

PATENT ABSTRACTS OF JAPAN

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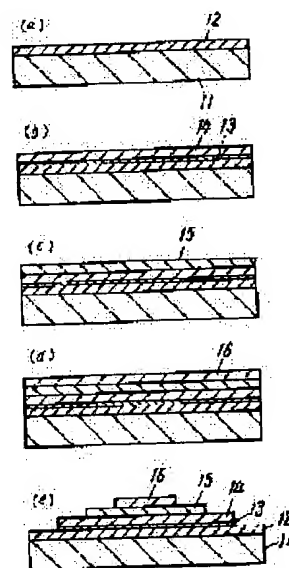
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(54) CAPACITANCE ELEMENT AND METHOD OF MANUFACTURING

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain a capacitance element without the peeling off of an adhering layer or the deterioration of an electric characteristic by suppressing the diffusion of the metal components of the adhering layer in the method of manufacturing the capacitance element with the capacitance insulating film of ferroelectric material.
 SOLUTION: An adhering layer 13 made of metal or metal oxide and a lower electrode 14 made of platinum are formed on a supporting substrate 11. Together with forming the capacitance insulating film 15 made of the metal oxide, an upper electrode 16 is formed. In the step of forming the lower electrode 14, the sputtering method is used to form the platinum film of the internal tensile stress of 2×10^9 dyne/cm² or less after the film forming by setting the temperature of the substrate at 200°C to 600°C, and forming the platinum film of dense film quality, the diffusion of the metal components of the adhered layer is suppressed, the peeling off of the adhesion layer is prevented and the deterioration of the electric characteristic is prevented.



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CLAIMS

[Claim(s)]

[Claim 1] Capacitative element characterized by having the up electrode which consisted of the metal or metallic oxide formed on the support substrate, was formed on the adhesion layer and this adhesion layer, and was formed on the capacity insulator layer which consists of a metallic oxide formed on the lower electrode which consists of platinum whose tensile stresses are two or more 2×10^9 dyn/cm, and this lower electrode, and this capacity insulator layer.

[Claim 2] The manufacture method of capacitative element characterized by providing the following. The process which forms the adhesion layer which consists of a metal or a metallic oxide on a support substrate. The process which uses argon gas, forms platinum by the sputtering method which set substrate temperature as 200 degrees C or more 600 degrees C or less, and forms a lower electrode on the aforementioned adhesion layer. The process which forms the capacity insulator layer which consists of a metallic oxide on the aforementioned lower electrode, and the process which forms an up electrode on the aforementioned capacity insulator layer.

[Claim 3] The manufacture method of the capacitative element according to claim 2 characterized by the sputtering method being the parallel flat-surface type magnetron direct-current electric-field sputtering method.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention relates to the capacitive element which makes the metallic oxide which has a ferroelectricity a capacity insulator layer, and its manufacture method.

[0002]

[Description of the Prior Art] ED for forming the capacitive element which makes the ferroelectric film which has a spontaneous-polarization property a capacity insulator layer on a semiconductor integrated circuit aiming at utilization of the nonvolatile RAM in which low operating voltage, high-speed writing, and high-speed read-out are possible is performed briskly. [0003] Hereafter, conventional capacitive element and its conventional manufacture method are explained using the process cross section of drawing 6.

[0004] As shown in drawing 6 (a), the silicon oxide used as the layer insulation film 2 is formed on the support substrate 1 which consists of a silicon substrate. Next, as shown in drawing 6 (b), the thickness used as the titanium metal and the lower electrode 4 whose thickness used as the adhesion layer 3 is about 20nm forms continuously the platinum which is 300nm by the sputtering method using argon gas at a room temperature on the layer insulation film 2. Next, as shown in drawing 6 (c), the ferroelectric film whose composition used as the capacity insulator layer 5 is $\text{SrBi}_2\text{Ta}_2\text{O}_9$ is applied by the spin turning-on method on the lower electrode 4, and it calcinates at 800 degrees C. Next, as shown in drawing 6 (d), the platinum used as the up electrode 6 is formed by the sputtering method on the capacity insulator layer 5. As furthermore shown in drawing 6 (e), it is processed by the photoetching method and the dry etching method, and capacitive element is formed.

[0005]

[Problem(s) to be Solved by the Invention] However, since it was the rude membraneous quality with which the columnar grain was located in a line since the platinum which forms the lower electrode 4 was formed at the room temperature in conventional structure and its conventional manufacture method, it was easy to diffuse the metal component of the adhesion layer 3 to the lower electrode 4 through the grain boundary, and it had the technical problem that the adhesion layer 3 disappears, adhesion intensity deteriorates, peeling arises, or it was further spread even in the capacity insulator layer 5, and the electrical property of capacitive element deteriorated.

[0006] It aims at offering capacitive element without peeling or electrical property degradation, and its manufacture method by this invention's solving the above-mentioned conventional technical problem, and forming precise membraneous platinum.

[0007]

[Means for Solving the Problem] In order to attain this purpose, the platinum which forms the lower electrode by which the capacitive element of this invention was formed on the adhesion layer makes substrate temperature 200 degrees C or more 600 degrees C or less for the platinum with which the manufacture method forms a lower electrode by having the internal stress of a two or more 2×10^9 dyn/cm tensile stress, and it forms by the sputtering method by argon gas.

[0008] According to this invention, precise membraneous platinum can be formed and capacitive element without peeling or electrical property degradation is obtained.

[0009]

[Embodiments of the Invention] Invention of this invention according to claim 1 consists of the metal or metallic oxide formed on the support substrate. An adhesion layer, The lower electrode which is formed on this adhesion layer and consists of platinum whose tensile stresses are two or more 2×10^9 dyn/cm, Since it has the up electrode formed on the capacity insulator layer which consists of a metallic oxide formed on this lower electrode, and this capacity insulator layer and platinum serves as precise membraneous quality by this, it has the operation which suppresses being spread to the lower electrode in which the metal component which forms an adhesion layer was formed with platinum.

[0010] The process at which invention according to claim 2 forms the adhesion layer which consists of a metal or a metallic oxide on a support substrate, The process which uses argon gas, forms platinum by the sputtering method which set substrate temperature as 200 degrees C or more 600 degrees C or less, and forms a lower electrode on the aforementioned adhesion layer, It has the process which forms an up electrode on the process which forms the capacity insulator layer which consists of a metallic oxide on the aforementioned lower electrode, and the aforementioned capacity insulator layer. The tensile stress of the platinum which forms a lower electrode by this can be made into two or more 2×10^9 dyn/cm, and platinum can be made into precise membraneous quality. The metal component which forms an adhesion layer as a result can suppress being spread to the lower

electrode formed with platinum.

[0011] The sputtering method according to claim 2 is the parallel flat-surface type magnetron direct-current electric-field sputtering method, and, thereby, invention according to claim 3 can make platinum more precise membrane quality.

[0012] Hereafter, the capacitive element in a gestalt and its manufacture method of 1 operation of this invention are explained using the process cross section of drawing 1.

[0013] (Gestalt 1 of operation) As shown in drawing 1 (a), the silicon oxide used as the layer insulation film 12 is formed on the support substrate 11 which consists of a silicon substrate. Next, as shown in drawing 1 (b), the titanium metal whose thickness used as the adhesion layer 13 is about 20nm is formed on the layer insulation film 12, and the thickness which serves as the lower electrode 14 on it sets substrate temperature as 200 degrees C - 600 degrees C, and forms the platinum which is 300nm by the parallel flat-surface type magnetron direct-current electric-field sputtering method using argon gas. Next, as shown in drawing 1 (c), the ferroelectric film whose composition used as the capacity insulator layer 15 is SrBi₂Ta₂O₉ is applied by the spin turning-on method on the lower electrode 14, and it calcinates at 800 degrees C. Next, as shown in drawing 1 (d), the platinum used as the up electrode 16 is formed by the sputtering method on this. As furthermore shown in drawing 1 (e), it is processed by the photoetching method and the dry etching method, and capacitive element is formed.

[0014] By the way, sputtering of the platinum which forms the lower electrode 14 of drawing 1 (b) requires precise membraneous platinum, in order to prevent the diffusion to the lower electrode 14 of the titanium metal of the adhesion layer 13. The relation between the membrane formation conditions of platinum and the internal stress of platinum is shown in drawing 2 - drawing 4. It becomes such a precise film that internal stress is large in the direction of hauling. This is explained below. Drawing 2 is a room temperature and is drawing showing Ar gas pressure dependency of the internal stress of the platinum in sputtering power 0.72kW conditions. Drawing 3 is a room temperature and is drawing showing the sputtering power dependency of the internal stress of the platinum in the conditions of Ar gas pressure 8mTorr. Drawing 4 is drawing in which Ar gas pressure shows the substrate temperature dependence of the internal stress of the platinum in the conditions of 8mTorr(s) by sputtering power 0.72kW. As shown in drawing, the internal stress of platinum is seldom changing depending on Ar gas pressure or sputtering power. Internal stress becomes strong in the direction of hauling, so that the internal stress of platinum has large substrate temperature dependence and substrate temperature is high compared with these. The substrate temperature dependence in the conditions whose Ar gas pressure of the adhesion intensity of the platinum of the lower electrode 14 after capacitive-element formation and the silicon oxide of the layer insulation film 12 formed on the support substrate 11 is 8mTorr(s) and sputtering power 0.72kW is shown in drawing 5. Adhesion intensity was evaluated as a critical load when a film peels by the scanned type scratch circuit tester. A critical load becomes large, so that substrate temperature is high. A critical load, i.e., adhesion intensity, is large, and this shows a bird clapper, so that the tensile stress of platinum becomes large. Consequently, diffusion of the titanium which forms the adhesion layer 13 is suppressed, adhesion intensity is strong and a bird clapper is known, so that the tensile stress of platinum will become large, if it puts in another way so that substrate temperature becomes high. The above result, by forming the precise film which makes it 200 degrees C or more with which the critical load which showed substrate temperature to drawing 5 is saturated mostly, and has a two or more 2×10^9 dyn/cm tensile stress, the membrane formation conditions of platinum can suppress titanium diffusion mostly, and can lose degradation of adhesion.

[0015] In addition, when making it 600 degrees C or more, the upper limit of substrate temperature was made into 600 degrees C because hillrock became easy to be made to that diffusion progresses too much or a metal membrane.

[0016] In addition, although considered as the mere silicon substrate as a support substrate with the form of this operation, the silicon substrate which made the integrated circuit is sufficient, or a quartz substrate, a GaAs substrate, etc. are sufficient. Moreover, with the form of this operation, as a capacity insulator layer, although SrBi₂Ta₂O₉ of typical composition which has Bi system stratified perovskite type structure was used, other ferroelectric films, such as Pb(Zr_{1-x}Ti_x)O₃ and TiO (Ba_{1-x}Sr_x)₃, are sufficient, or other metallic oxides, such as a tantalic-acid ghost, are sufficient.

[0017] Moreover, although the capacity insulator layer was formed by the spin turning-on method with the form of this operation, you may form by the sputtering method or the chemical-vapor-deposition method.

[0018] Moreover, although titanium metal was used for the adhesion layer with the form of this operation, other metallic oxides, such as other metals, such as a tantalum, and a ruthenium oxide, an iridium oxide, are sufficient.

[0019]

[Effect of the Invention] The capacitive element of this invention is that in which the platinum which forms a lower electrode has the internal stress of two or more 2×10^9 dyn/cm hauling stress. It is characterized by the manufacture method forming this platinum at the substrate temperature of 200 degrees C - 600 degrees C by the sputtering method. When this forms precise membraneous platinum, it can prevent suppressing the diffusion by the side of a lower electrode, and an adhesion layer being thin, and the metal component of peeling or an adhesion layer by the bird clapper diffusing the metal component of an adhesion layer even in a capacity insulator layer, and degrading the electrical property of a capacity insulator layer.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The process cross section showing the capacitive element in a gestalt and its manufacture method of 1 operation of this invention

[Drawing 2] Drawing showing the argon gas pressure dependency of the internal stress of platinum

[Drawing 3] Drawing showing the sputtering power dependency of the internal stress of platinum

[Drawing 4] Drawing showing the substrate temperature dependence of the internal stress of platinum

[Drawing 5] Drawing showing the substrate temperature dependence of the adhesion of a platinum lower electrode and a support substrate

[Drawing 6] The process cross section showing the manufacture method of the capacitive element in the conventional example

[Description of Notations]

11 Support Substrate

12 Layer Insulation Film

13 Adhesion Layer

14 Lower Electrode

15 Capacity Insulator Layer

16 Up Electrode

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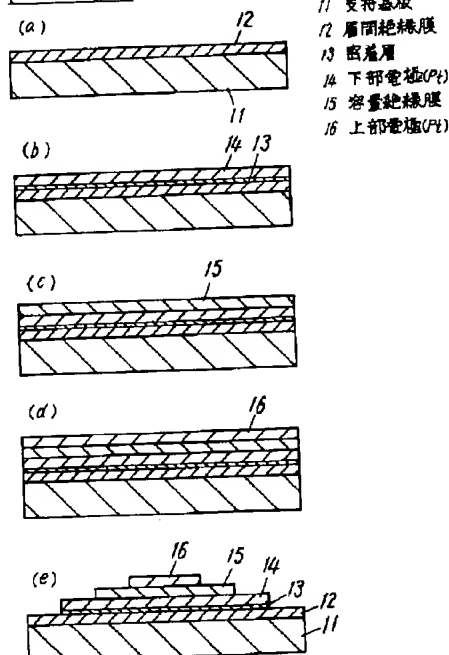
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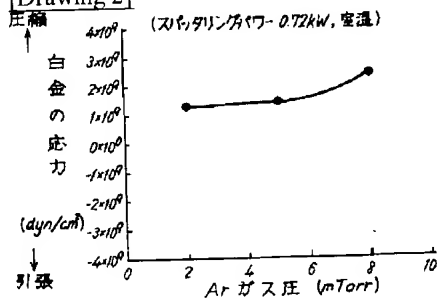
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DRAWINGS

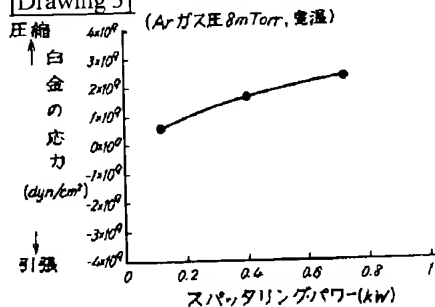
[Drawing 1]



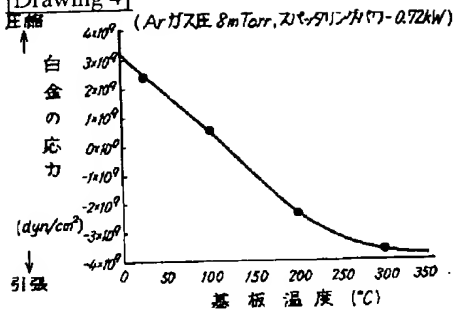
[Drawing 2]



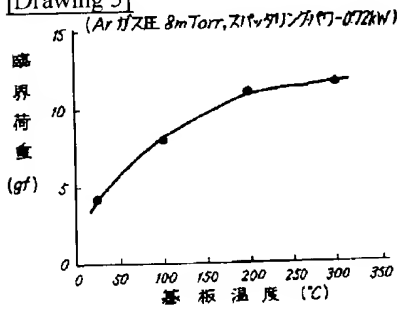
[Drawing 3]



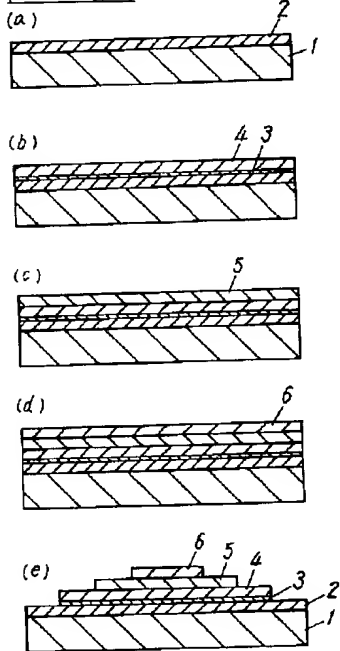
[Drawing 4]



[Drawing 5]



[Drawing 6]



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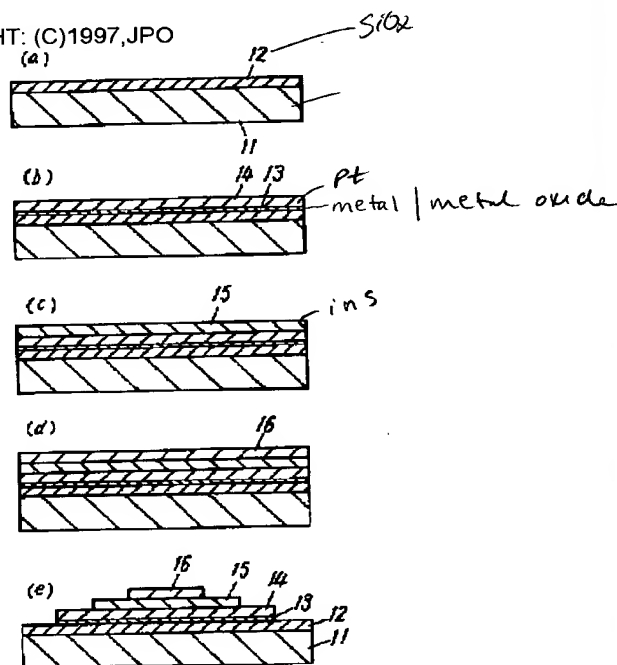
H01G 4/10**H01G 4/012**(21) Application number: **08055733**(22) Date of filing: **13.03.96**(71) Applicant: **MATSUSHITA ELECTRON CORP**(72) Inventor:
NASU TORU
IZUTSU YASUFUMI
KIBE MAKI**(54) CAPACITANCE ELEMENT AND METHOD OF MANUFACTURING****(57) Abstract:**

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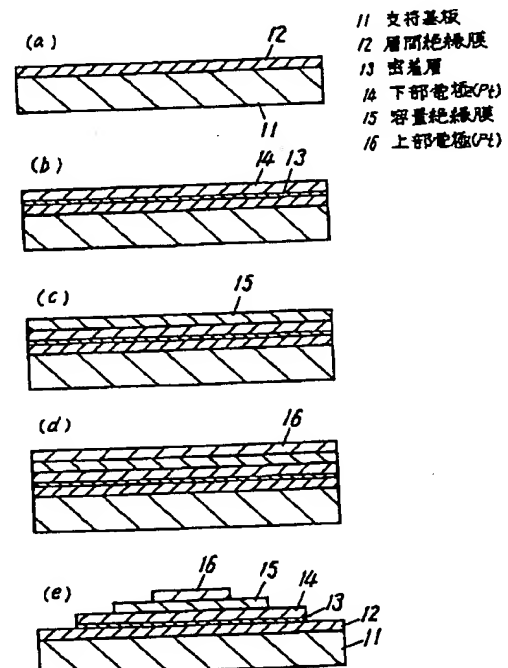
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(54) 【発明の名称】 容量素子およびその製造方法

(57) 【要約】

【課題】 強誘電体膜を容量絶縁膜とする容量素子の製造方法において、密着層の金属成分の拡散を抑制し、はがれや電気的特性劣化のない容量素子を得ることを目的とする。

【解決手段】 支持基板11上に金属または金属酸化物よりなる密着層13を形成する工程と、白金よりなる下部電極14を形成する工程と、金属酸化物よりなる容量絶縁膜15を形成する工程と、上部電極16を形成する工程とを備え、下部電極14を形成する工程が、成膜後で $2 \times 10^9 \text{ dyn/cm}^2$ 以下の引っ張り応力の内部応力を有する白金を形成するために基板温度を $200^\circ\text{C} \sim 600^\circ\text{C}$ に設定してスパッタリング法により形成することを特徴とし、緻密な膜質の白金を形成することにより、密着層の金属成分の拡散を抑制し、はがれや電気的特性劣化を生じさせない。



【特許請求の範囲】

【請求項1】 支持基板上に形成された金属または金属酸化物よりなり密着層と、同密着層上に形成され、引っ張り応力が $2 \times 10^9 \text{ dyn/cm}^2$ 以上である白金よりなる下部電極と、同下部電極上に形成された金属酸化物よりなる容量絶縁膜、および同容量絶縁膜上に形成された上部電極とを備えたことを特徴とする容量素子。

【請求項2】 支持基板上に金属または金属酸化物よりなる密着層を形成する工程と、前記密着層上に、アルゴンガスをを用い、基板温度を 200°C 以上 600°C 以下に設定したスパッタリング法により白金を形成して下部電極を形成する工程と、前記下部電極上に金属酸化物よりなる容量絶縁膜を形成する工程、および前記容量絶縁膜上に上部電極を形成する工程とを備えたことを特徴とする容量素子の製造方法。

【請求項3】 スパッタリング法が平行平面型マグネトロン直流電界スパッタリング法であることを特徴とする請求項2記載の容量素子の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】 本発明は、強誘電性を有する金属酸化物を容量絶縁膜とする容量素子およびその製造方法に関する。

【0002】

【従来の技術】 低動作電圧、高速書き込みおよび高速読み出し可能な不揮発性RAMの実用化を目指し、自発分極特性を有する強誘電体膜を容量絶縁膜とする容量素子を半導体集積回路の上に形成するための技術開発が盛んに行われている。

【0003】 以下、従来の容量素子およびその製造方法を図6の工程断面図を用いて説明する。

【0004】 図6(a)に示すように、シリコン基板よりなる支持基板1上に層間絶縁膜2となるシリコン酸化膜を形成する。次に図6(b)に示すように、層間絶縁膜2の上に密着層3となる膜厚が約 20 nm の金属チタンおよび下部電極4となる膜厚が 300 nm の白金を、室温で、アルゴンガスをを用いたスパッタリング法により連続して形成する。次に図6(c)に示すように下部電極4の上に容量絶縁膜5となる組成が $\text{SrBi}_2\text{Ta}_2\text{O}_9$ である強誘電体膜をスピノン法で塗布し 800°C で焼成する。次に図6(d)に示すように容量絶縁膜5の上に上部電極6となる白金をスパッタリング法により形成する。さらに図6(e)に示すように写真食刻法とドライエッチング法により加工を行い、容量素子を形成する。

【0005】

【発明が解決しようとする課題】 しかしながら従来の構造およびその製造方法では、下部電極4を形成する白金を室温で形成しているため、柱状結晶粒の並んだ荒い膜質であるため結晶粒界を通じて密着層3の金属成分が、

下部電極4へ拡散し易く、密着層3が消滅して密着強度が劣化しはがれが生じたり、さらに容量絶縁膜5にまで拡散して容量素子の電気的特性が劣化するという課題を有していた。

【0006】 本発明は上記の従来の課題を解決するもので、緻密な膜質の白金を形成することにより、はがれや電気的特性劣化のない容量素子およびその製造方法を提供することを目的とする。

【0007】

【課題を解決するための手段】 この目的を達成するために本発明の容量素子は、密着層の上に形成された下部電極を形成する白金が、 $2 \times 10^9 \text{ dyn/cm}^2$ 以上の引っ張り応力の内部応力を有するものであり、その製造方法は、下部電極を形成する白金を基板温度を 200°C 以上 600°C 以下にしてアルゴンガスによるスパッタリング法により形成するものである。

【0008】 本発明によれば、緻密な膜質の白金を形成することができ、はがれや電気的特性劣化のない容量素子が得られる。

【0009】

【発明の実施の形態】 本発明の請求項1に記載の発明は、支持基板上に形成された金属または金属酸化物よりなり密着層と、同密着層上に形成され、引っ張り応力が $2 \times 10^9 \text{ dyn/cm}^2$ 以上である白金よりなる下部電極と、同下部電極上に形成された金属酸化物よりなる容量絶縁膜および同容量絶縁膜上に形成された上部電極とを備えたものであり、これにより白金が緻密な膜質となるため、密着層を形成する金属成分が白金で形成された下部電極へ拡散することを抑制する作用を有する。

【0010】 請求項2に記載の発明は、支持基板上に金属または金属酸化物よりなる密着層を形成する工程と、前記密着層上に、アルゴンガスをを用い、基板温度を 200°C 以上 600°C 以下に設定したスパッタリング法により白金を形成して下部電極を形成する工程と、前記下部電極上に金属酸化物よりなる容量絶縁膜を形成する工程および前記容量絶縁膜上に上部電極を形成する工程とを備えたものであり、これにより下部電極を形成する白金の引っ張り応力を $2 \times 10^9 \text{ dyn/cm}^2$ 以上とすることができ、白金を緻密な膜質とすることができる。この結果密着層を形成する金属成分が白金で形成された下部電極へ拡散することを抑制することができる。

【0011】 請求項3に記載の発明は、請求項2記載のスパッタリング法が平行平面型マグネトロン直流電界スパッタリング法であり、これにより白金をより緻密な膜質とすることができる。

【0012】 以下、本発明の一実施の形態における容量素子およびその製造方法を図1の工程断面図を用いて説明する。

【0013】 (実施の形態1) 図1(a)に示すように、シリコン基板よりなる支持基板11上に層間絶縁膜

12となるシリコン酸化膜を形成する。次に、図1

(b)に示すように、層間絶縁膜12の上に密着層13となる膜厚が約20nmの金属チタンを形成し、その上に下部電極14となる膜厚が300nmの白金を、基板温度を200℃～600℃に設定し、アルゴンガスを用いた平行平面型マグネトロン直流電界スパッタリング法により形成する。次に図1(c)に示すように下部電極14の上に容量絶縁膜15となる組成が $\text{SrBi}_2\text{Ta}_2\text{O}_9$ である強誘電体膜をスピノン法で塗布し800℃で焼成する。次に図1(d)に示すようにこの上に上部電極16となる白金をスパッタリング法により形成する。さらに図1(e)に示すように写真食刻法とドライエッチング法により加工を行い、容量素子を形成する。

【0014】ところで図1(b)の下部電極14を形成する白金のスパッタリングでは、密着層13の金属チタンの下部電極14への拡散を防ぐため緻密な膜質の白金が要求される。図2～図4に白金の成膜条件と白金の内部応力との関係を示す。内部応力が引っ張り方向で大きいほど緻密な膜となる。このことを以下に説明する。図2は室温で、スパッタリング・パワー0.72kWの条件での白金の内部応力のArガス圧依存性を示す図である。図3は室温で、Arガス圧8mTorrの条件での白金の内部応力のスパッタリング・パワー依存性を示す図である。図4はスパッタリング・パワー0.72kWでArガス圧が8mTorrの条件での白金の内部応力の基板温度依存性を示す図である。図から分かるように、白金の内部応力はArガス圧やスパッタリング・パワーによってはあまり変化していない。これらに比べて白金の内部応力は基板温度依存性が大きく、基板温度が高いほど内部応力は引っ張り方向に強くなる。図5に、容量素子形成後の下部電極14の白金と支持基板11上に形成された層間絶縁膜12のシリコン酸化膜との密着強度のArガス圧が8mTorr、スパッタリング・パワー0.72kWの条件での基板温度依存性を示す。密着強度は走査型スクラッチテストにより膜がはがれた時の臨界荷重として評価した。基板温度が高いほど臨界荷重が大きくなる。このことから白金の引っ張り応力が大きくなるほど、臨界荷重すなわち密着強度が大きくなることわかる。この結果、基板温度が高くなるほど、言い換えれば白金の引っ張り応力が大きくなるほど、密着層13を形成するチタンの拡散が抑制され、密着強度が強くなることわかる。以上の結果、白金の成膜条件は基板温度を図5に示した臨界荷重がほぼ飽和する200℃以上にして $2 \times 10^9 \text{ dyn/cm}^2$ 以上の引っ張り応力を有する緻密な膜を形成することにより、チタン拡散をほぼ抑制し、密着性の劣化をなくすることができる。

【0015】なお基板温度の上限を600℃としたの

は、600℃以上にすれば拡散が進みすぎることや金属膜にヒルロックができやすくなるためである。

【0016】なお本実施の形態では支持基板として単なるシリコン基板としたが、集積回路を作り込んだシリコン基板でもよく、あるいは石英基板やGaAs基板などでもよい。また本実施の形態では容量絶縁膜として、Bi系層状ペロブスカイト型構造を有する代表的な組成の $\text{SrBi}_2\text{Ta}_2\text{O}_9$ を用いたが $\text{Pb}(\text{Zr}_{1-x}\text{Ti}_x)\text{O}_3$ や $(\text{Ba}_{1-x}\text{Sr}_x)\text{TiO}_3$ などの他の強誘電体膜でもよく、あるいはタンタル酸化物などの他の金属酸化物でもよい。

【0017】また本実施の形態では容量絶縁膜をスピノン法で形成したが、スパッタリング法や化学気相成長法で形成してもよい。

【0018】また本実施の形態では密着層に金属チタンを用いたが、タンタルなどの他の金属やルテニウム酸化物・イリジウム酸化物などの他の金属酸化物でもよい。

【0019】

【発明の効果】本発明の容量素子は、下部電極を形成する白金が $2 \times 10^9 \text{ dyn/cm}^2$ 以上の引っ張り応力の内部応力を有するものであり、その製造方法はこの白金をスパッタリング法により200℃～600℃の基板温度で形成することとを特徴とし、これにより緻密な膜質の白金を形成することにより密着層の金属成分を下部電極側への拡散を抑制し、密着層が薄くなることによるはがれや密着層の金属成分が容量絶縁膜にまで拡散してきて容量絶縁膜の電気的特性を劣化させることを防ぐことができる。

【図面の簡単な説明】

【図1】本発明の一実施の形態における容量素子およびその製造方法を示す工程断面図

【図2】白金の内部応力のアルゴンガス圧依存性を示す図

【図3】白金の内部応力のスパッタリング・パワー依存性を示す図

【図4】白金の内部応力の基板温度依存性を示す図

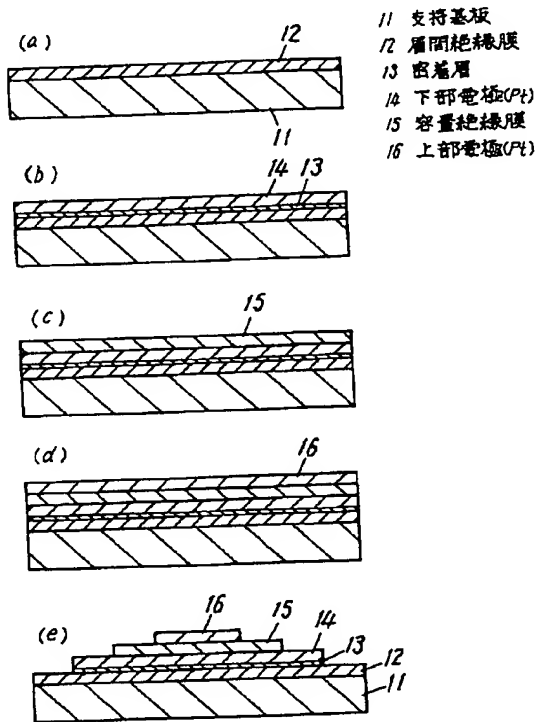
【図5】白金下部電極と支持基板との密着性の基板温度依存性を示す図

【図6】従来例における容量素子の製造方法を示す工程断面図

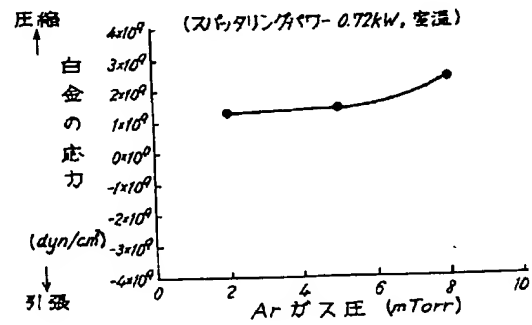
【符号の説明】

- 11 支持基板
- 12 層間絶縁膜
- 13 密着層
- 14 下部電極
- 15 容量絶縁膜
- 16 上部電極

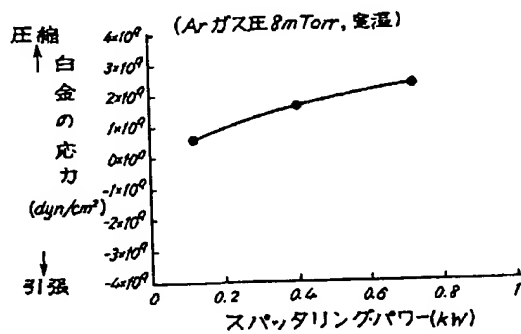
【図1】



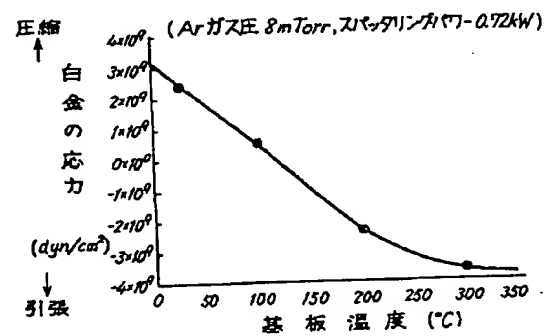
【図2】



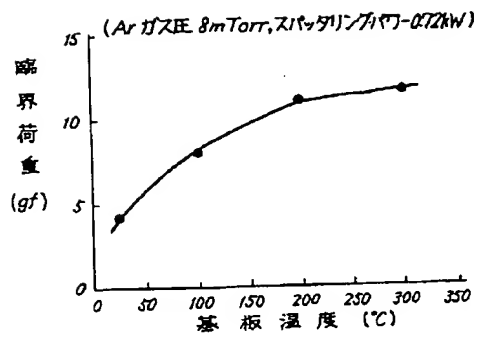
【図3】



【図4】



【図5】



【図6】

